CLAIMS

1. A data processing device including:

a processor;

a charge storage device coupled to the processor; and

a current source for supplying the processor with operating current, and adapted to vary its output current independently of the instantaneous power demand of the processor.

2. The device of claim 1 in which the charge storage device comprises a capacitor in series with the current source, and across which the processor is connected in parallel.

3. The device of claim 1 or claim 2 in which the current source is adapted to periodically or aperiodically switch between two different current levels.

4. The device of claim 1 or claim 2 in which the current source is adapted to periodically or aperiodically switch between multiple current levels.

5. The device of claim 3 or claim 4 in which the interval between switching current levels is determined by an average power demand of the processor.

6. The device of claim 1 in which the current source comprises:

a first current source adapted to provide substantially constant current at at least two different current levels, the first current source switching between current levels on a periodic or aperiodic basis; and

a second current source adapted to provide a noise current that varies on a random or pseudo-random basis.

7. The device of any preceding claim further including control means adapted to maintain the supply voltage to the processor between an upper voltage limit and a lower voltage limit.

8. The device of any preceding claim further including a zener diode adapted to maintain the supply voltage to the processor below an upper voltage limit.

9. The device of claim 7 in which the control means includes current switching means for switching the current source between a first, higher current level and a second, lower current level, the current switching being triggered by the supply voltage to the processor respectively reaching the lower voltage limit and the upper voltage limit.

10. The device of claim 9 further including a timer for determining a time period taken for the processor supply voltage to reach a lower voltage limit from an upper voltage limit, or vice versa.

11. The device of claim 10 further including current setting means for varying the first current level and / or the second current level of the current source if the timer determines that the time period falls outside predetermined limits.

12. The device of claim 11 in which the current setting means raises the first current level if the timer determines that the time period for reaching the lower voltage limit falls below a first predetermined threshold.

13. The device of claim 11 or claim 12 in which the current setting means reduces the first current level if the timer determines that the time period for reaching the lower voltage limit exceeds a second predetermined threshold.

14. The device of claim 11 in which the current setting means reduces the second current level if the timer determines that the time period for reaching the upper voltage limit falls below a first predetermined threshold.

15. The device of claim 11 or claim 12 in which the current setting means raises the second current level if the timer determines that the time period for reaching the upper voltage limit exceeds a second predetermined threshold.

16. The device of claim 9 in which the control means includes means for temporarily inhibiting the current switching means if the supply voltage to the processor fails to move towards the desired upper or lower voltage limit.

17. The device of claim 1 in which the processor has an internal clock, the frequency of which is dependent upon the supply voltage to the processor.

18. The device of any preceding claim in which the processor is a cryptographic processor.

19. The device of any preceding claim incorporated into a smart card.

20. A method of operating a data processing device, comprising the steps of:

drawing current from an external supply;

cyclically apportioning drawn current between a charge storage device and a processor within the data processing device such that the drawn current varies independently of the instantaneous power demand of the processor.

21. The method of claim 20 further including the step of using the drawn current to generate a current flow to the processor and the charge

storage device, that is periodically or aperiodically switched between two different current levels.

22. The method of claim 20 further including the step of using the drawn current to generate a current flow to the processor and the charge storage device, that is periodically or aperiodically switched between multiple different current levels.

23. The method of claim 21 or claim 22 further including the step of determining the interval between switching according to an average power demand of the processor.

24. The method of claim 20 further including the steps of:

using a first current source to deliver substantially constant current at at least two different current levels, switching the first current source between current levels on a periodic or aperiodic basis;

using a second current source to provide a superposed current that varies on a random or pseudo-random basis and

delivering the combined current of the first and second current sources to the processor and the charge storage device.

25. The method of any one of claims 20 to 24 further including the step of maintaining a supply voltage to the processor between an upper voltage limit and a lower voltage limit.

26. The method of claim 25 further including the step of switching a current source between a first, higher current level and a second, lower current level, when the supply voltage to the processor respectively reaches the lower voltage limit and the upper voltage limit.

27. The method of claim 26 further including the steps of:

determining a time period taken for the processor supply voltage to reach a lower voltage limit from an upper voltage limit, or vice versa, and

varying the first current level and / or the second current level of the current source if the time period falls outside predetermined limits.

28. The method of claim 27 further including the step of raising the first current level if the time period for reaching the lower voltage limit falls below a first predetermined threshold.

29. The method of claim 27 or claim 28 further including the step of reducing the first current level if the time period for reaching the lower voltage limit exceeds a second predetermined threshold.

30. The method of claim 27 further including the step of reducing the second current level if the time period for reaching the upper voltage limit falls below a first predetermined threshold.

31. The method of claim 27 or claim 28 further including the step of raising the second current level if the time period for reaching the upper voltage limit exceeds a second predetermined threshold.

32. The method of claim 26 further including the step of temporarily inhibiting the current switching if the supply voltage to the processor fails to move towards the desired upper or lower voltage limit.

33. The method of claim 20 further including the step of controlling the frequency of operation of the processor as a function of the supply voltage to the processor.

34. A data processing device substantially as described herein with reference to the accompanying drawings.

35. A method of operating a data processing device substantially as described herein with reference to the accompanying drawings.